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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No.	32809
First Inventor or Application Identifier	Kenji Shimazaki
Title	METHOD OF ANALYZING ELECTROMAGNETIC...
Express Mail Label No.	EL633643636US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

1. [X] * Fee Transmittal Form *(e.g., PTO/SB/17)* *(Submit an original and a duplicate for fee processing)*
2. [X] Specification [Total Pages 32]
   (preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 U.S.C. 113)* [Total Sheets 22]
4. Oath or Declaration [Total Pages 3]
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 C.F.R. § 1.63(d)) *(for continuation/divisional with Box 16 completed)*
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

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6. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
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7. [X] Assignment Papers (cover sheet & document(s))
8. [ ] 37 C.F.R.§3.73(b) Statement *(when there is an assignee)* [X] Power of Attorney
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PATENT

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Sir:

Transmitted herewith for filing by other than a small entity is the patent application of:

Inventor: Kenji Shimazaki, Hiroyuki Tsujikawa, Seijirou Kojima, and Shouzou Hirano

For: METHOD OF ANALYZING ELECTROMAGNETIC INTERFERENCE

22 sheets of informal drawings are included.

An assignment of the invention to Matsushita Electric Industrial Co., Ltd. is included along with a Recordation Form Cover Sheet. Please record and return the assignment to the undersigned.

Priority is claimed under 35 U.S.C. §119 on the basis of the following foreign applications:

Japanese Patent Application No. Hei. 11-200847 Filed July 14, 1999

A certified copy of this application is enclosed.

An Information Disclosure Statement is enclosed.

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The Commissioner is hereby authorized to charge any fees under 37 C.F.R. §§1.16 and 1.17 which may be required during the entire pendency of this application, or to credit any overpayment, to Deposit Account No. 16-0820, Order No. 32809.

Respectfully,

PEARNE & GORDON LLP

David E. Spaw, Reg. No. 34732

Date: July 13, 2000

METHOD OF ANALYZING ELECTROMAGNETIC INTERFERENCE

Background of the Invention

1.Field of the Invention

The present invention relates to a method of analyzing electromagnetic interference (EMI) (hereinafter often referred to as an "EMI analysis method"), and more particularly, to a method of analyzing electromagnetic interference arising in a large-scale, high-speed LSI (large-scale integrated circuit) by means of high-speed, highly-accurate logic simulation.

2.Description of the related Art

LSIs find a broadening range of applications, from communications devices, such as cellular phones, to general household products, toys, and automobiles, as well as applications in the field of computers. Electromagnetic interference arising in such a product induces radio interference noise in a receiver, such as a TV set or a radio, or faulty operations of another system. In order to prevent this problem, the entirety of a product is shielded, or filters are provided in a product. With a view towards preventing an increase in the number of components and cost and difficulty in preventing occurrence of electromagnetic interference in a product, strong demand exists for suppression of noise in an LSI itself.

Under such a situation, an LSI is ranked as a key device for any product which contains an LSI. Demand exists for an larger-scale, high-speed LSI for ensuring competitiveness of a product. In a situation in which the cycle of product development becomes shorter, design-automation of an LSI is indispensable for satisfying the demand. There is growing necessity for adopting synchronous circuit as a condition for introducing a state-of-the-art design-automation method. In a case where all circuits of a large-scale, high-speed LSI operate synchronously with a reference clock signal, instantaneously-changing current becomes very large and induces an increase in electromagnetic interference.

The present invention relates to a simulation method which enables evaluation of EMI indispensable for reducing electromagnetic interference while maintaining a tendency toward a larger-scale, higher-speed LSI.

Noise imposed on another device by an LSI is roughly classified into two types; radiation noise, and conduction noise. Radiation noise emanated directly from an LSI includes noise emitted from internal wires of an LSI. However, internal wires do not act as an antenna of large size. As a matter of course, it is considered that the noise emitted directly from an LSI will pose a problem in the future, in association with an improvement in the operation frequency of an LSI. However, as of now, the noise emitted from the inside of an LSI is

considered trivial.

In contrast, conduction noise affects another device mounted on a printed board, by way of direct interconnections, such as wires of an LSI or routings provided on a printed wiring board. Noise is emitted from such interconnections while the interconnections are act as the source of origination or as an antenna. The antenna constituted of the interconnections is much larger than that constituted by internal wires of an LSI and is a dominant element in terms of electromagnetic emission.

A power line and a signal line can act as paths along which conduction noise developing in an LSI travels. In consideration of an electromagnetic field in the vicinity of an LSI, noise which results from variation in an electric current of a power source being emitted from a power line serving as an antenna is considered to be dominant. There may be a case where ringing and overshoot phenomena stemming from variation in a signal pose problems. However, there more frequently arises a case where variation in an internal power level of an LSI propagates as a signal waveform, to thereby present a problem. Noise emitted from a power line or a signal line is considered to have a strong correlation with variation in the electric current of a power source (hereinafter referred to as a "source current").

A source current of a CMOS circuit will now be described by reference to a simple inverter circuit. In a case where variation arises in a voltage applied to an inverter circuit, there flows a load capacity charge/discharge current, which is the primary source current of the CMOS circuit. In addition, a short circuit current flows together with the load capacity charge/discharge current. In design of such a CMOS circuit, all circuits of an LSI are synchronized in accordance with constraints on the use of a design-automation tool. As a result of all circuits being synchronized, all circuits of the LSI operate simultaneously, and a peak current arises in a power source in synchronism with a reference clock signal. Further, in order to increase operating speed, or shorten a cycle, of the LSI, the capacity of a transistor is increased so as to enable a charging/discharging operation to be completed within a short period of time. Eventually, a peak current increases. As a matter of course, the total source current of an LSI is increased when the level of an LSI is increased. Thus, the peak current of the power source is increased, thereby inducing occurrence of an abrupt change in a source current. Such an abrupt change induces an increase in higher harmonic components, thereby resulting in an increase in electromagnetic interference.

Highly-precise simulation of change in a source current, which may be said to primarily account for electromagnetic

interference, is considered to be effective in evaluation of electromagnetic interference arising in an LSI.

A current simulation method for effecting transistor-level current analysis, as will be described below, has conventionally been employed.

FIG. 15 is a block diagram showing the flow of processing operations pertaining to a conventional transistor-level EMI analysis method. According to this method, on the basis of layout information pertaining to an LSI which is to be analyzed through use of a transistor-level current analysis method, there is performed layout parameter extraction (hereinafter referred to simply as an "LPE") processing 03. Subsequently, there is performed circuit simulation 06 regarding a switch-level netlist; source-of-current modeling 08; a power line LPE step 010; transient analysis simulation 012; and FFT processing 014.

Processing pertaining to each of the foregoing processing steps will now be described by reference to FIG. 15.

First, in step 03 are input layout data 01 pertaining to a semiconductor integrated circuit to be subjected to EMI analysis; parameters of elements, such as transistor elements or various parasitic wiring elements (e.g., resistors and capacitors); and an LPE rule 02 for defining a form in which extracted layout parameters are to be output. In accordance

with the LPE rule 02, parameters of the respective elements included in the layout data 01 are calculated, whereby a netlist 04 is produced. In step 03, parasitic elements of a power source (and the ground) are not objects of extraction.

In step 06 are input the netlist 04 prepared in step 03 and a test pattern 05 for causing a circuit, which serves as an object of analysis, to replicate a desired logic operation. There are calculated a load capacity charge/discharge current and a short circuit current, which correspond to the operating state of an internal circuit, thereby producing current waveform information 07 concerning the waveform of an electric current of a transistor. The first operation of the processing pertaining to step 06 is effected on the assumption that the potential of a power source (and that of ground) is a variation-free, ideal potential.

In step 08 is entered the current waveform information 07 concerning a transistor prepared in step 06. The thus-entered current waveform information 07 is modeled into a mode which can be applied to subsequent step 012, wherewith current source element model information 09 is prepared. In order to alleviate a load which would be imposed on subsequent step 012, a function circuit block consisting of a plurality of transistors is usually modeled as a single current-source element.

Processing pertaining to step 010 differs from

processing pertaining to step 03, only in that rather than parameters of transistor elements and those of various parasitic wiring elements, parameters of parasitic elements of a power source and those of a ground wire (e.g., resistors, decoupling capacitance, and like elements) are taken as objects of extraction. Hence, repeated explanation is omitted. In step 010, a power source (and ground) wiring netlist 011 is produced.

In step 012 are entered the current source element model information 09 prepared in step 08, the power source (and ground) wiring netlist 011 prepared in step 010, and impedance 016 of a wire or a lead frame (including, resistance, capacitance, and inductance). Through analysis of these input data carried out by a transient analysis simulator typified by SPICE, fluctuations in line voltage of a circuit to be analyzed are calculated. Thus, there is produced a line voltage drop result 017 concerning the thus-calculated fluctuations in line voltage.

Subsequently, processing pertaining to step 06 is performed again. In contrast with the first operation of the processing pertaining to step 06 having been effected on the assumption that the potential of the power source (and the ground) is a fluctuation-free, ideal potential, the line voltage drop result 017 prepared in step 012 is entered. The current waveform information 07 concerning a transistor is

prepared again in consideration of fluctuations in line voltage. Similarly, processing pertaining to steps 08 and 012 is repeated.

Processing pertaining to steps 06, 08, and 012 is effected several times in a looped manner, wherewith there is produced a current waveform result 013 which highly-accurately duplicates fluctuations in line voltage.

In step 014, the current waveform result 013 prepared in step 012 is entered and subjected to fast Fourier transformation (hereinafter abbreviated FFT), to thereby enable frequency spectrum analysis. There is obtained an EMI analysis result 015.

In the conventional example, the precision of verification varies greatly according to combination of the LPE processing 03, the power line LPE processing 010, and the source current modeling processing 08. However, a certain level of accuracy of analysis can be expected. A transient analysis simulator typified by SPICE is used for transistor-level analysis of an electric current. Hence, a limitation is imposed on the level of a circuit to be analyzed, and an enormous amount of processing time is required. The level of a semiconductor integrated circuit has increased recently, and establishment of an EMI analysis method which enables high-speed analysis of an electric current on a level larger than a transistor level is desired.

A gate-level current analysis method has conventionally been proposed as a current analysis method which can be made faster. This gate-level current analysis method is used for analyzing power consumption. One example of a gate-level current analysis method is EMI-noise analysis which is to be effected in an ASIC design environment. The method is described in "EMI-Noise Analysis Under ASIC Design Environment" (ISPD&99, pp. 16 through 21). According to this technique, an event is acquired from the result of a gate-level simulation using a test vector, and the waveform of an electric current is estimated. The frequency of the thus-estimated current waveform is analyzed through fast Fourier transformation (FFT). More specifically, as shown in FIG. 16, a logic simulation 104 is effected on the basis of a netlist 101 and a test vector 102, wherewith event information 105 is calculated. On the basis of the thus-calculated event information 105 and waveform information 103 obtained at the time of toggling, processing pertaining to a current waveform calculation section 107 is executed, to thereby produce a current waveform calculation result 108. This current waveform calculation result 108 is subjected to FFT processing 109, to thereby produce a frequency characteristic 110. The EMI-noise analysis method can effect an EMI analysis operation faster than that performed according to the conventional gate - level EMI analysis method. However, use of a test vector

still involves consumption of much execution time. Therefore, the processing speed achieved by the EMI-noise analysis method is not sufficiently high, and demand still exists for an increase in processing speed of the EMI-noise analysis method. The EMI-noise analysis method also encounters a problem of an analysis result being dependent on the pattern of an employed test vector.

As mentioned above, the conventional example using the transistor-level current analysis method can be expected to yield a certain level of accuracy. However, a transient analysis simulator typified by SPICE is used for transistor-level current analysis. A limitation is imposed on the level of a circuit to be analyzed, and an enormous amount of processing time is required. The level of a semiconductor integrated circuit has increased recently, and there is desired establishment of an EMI analysis method which enables high-speed analysis of an electric current at a scale larger than the scale which can be analyzed by a transistor-level simulator.

The gate-level simulation using a test vector has also been proposed. However, the example conventional gate-level simulation technique encounters difficulty in increasing the speed of analysis. Since the gate-level simulation technique employs a test vector, an analysis result is dependent on the

employed test pattern.

Summary of the Invention

The present invention has been conceived to solve the drawbacks of the conventional methods and is aimed at evaluating electromagnetic interference developing in an LSI through a simulation by means of high-speed, highly-accurate analysis of a power-supply current.

To this end, the present invention provides a method of analyzing electromagnetic interference (an EMI analysis method). In contrast with a known dynamic gate-level simulation method, the EMI analysis method enables estimation of EMI noise, by means of calculating signal propagation of each node through use of the signal propagation probability technique, and calculating variation time of each node through use of "the Static timing analysis technique". In short, the present invention is characterized in calculating a frequency characteristic from the relationship between toggle probability of each node and delay in each node.

More specifically, the present invention provides a method of analyzing electromagnetic interference generating in an LSI, comprising:

a correction step of correcting the amplitude of a current estimation waveform in each node which has been previously prepared for each change in each node, in accordance with the probability of variation in each node;

an addition step of adding current waveforms of all nodes together within a period of time corresponding to one cycle, provided that the thus-corrected current waveform appears at a time a signal arrives at each node; and

a frequency analysis step of analyzing the frequency of the current waveform calculated in the addition step.

The probability of variation in each node is calculated through use of the signal propagation probability technique. Further, the time at which a signal arrives at each node is calculated through use of the static timing analysis technique. The time at which a signal arrives is defined so as to fall within the range between the maximum time and the minimum time, in accordance with an average time, the maximum time, the minimum time, or a predetermined distribution such as a normal distribution.

Preferably, in the correction step, the amplitude of a current estimation waveform, which has been prepared for each change in each node, is corrected in accordance with the probability of variation in each node and a distribution with respect to time (hereinafter called "chronological distribution").

More specifically, the probability of change in each node is calculated through use of the signal propagation probability technique, and the chronological distribution at which a signal arrives at each node is calculated through use of the static

timing analysis technique.

Preferably, each node has a plurality of paths, and a current waveform is calculated in consideration of a case where each of the paths has a unique probability of change and signal arrival time.

Further, the present invention provides a method of analyzing electromagnetic interference developing in an LSI, the method comprising:

a waveform formation step of forming a current estimation waveform which has been prepared for each change in each node, as if the waveform randomly arises within a plurality of predetermined cycles, in accordance with the probability of change in each node and a time at which a signal arrives at each node;

adding the thus-prepared current estimation waveforms of all nodes, to thereby derive a current waveform; and

analyzing the frequency of the current waveform, thereby determining a noise characteristic of EMI.

In other words, under the EMI analysis method according to the present invention, the probability of change in each node is calculated through use of the signal propagation probability technique, and the result of calculation is stored as a probability at which a signal randomly changes. Further, a time at which a signal arrives at each node is calculated through use of the static timing analysis technique.

Moreover, the present invention provides a method of analyzing electromagnetic interference developing in an LSI, the method comprising:

a waveform formation step of forming a current estimation waveform which has been prepared for each change in each node, as if the waveform randomly arises within a plurality of predetermined cycles, in accordance with the probability of change in each node and chronological distribution probability;

adding the thus-prepared current estimation waveforms of all nodes, to thereby derive a current waveform; and

analyzing the frequency of the current waveform, thereby determining a noise characteristic of EMI.

More specifically, the probability of change in each node is calculated through use of the signal propagation probability technique, and the result of calculation is stored as the probability of a signal changing randomly. A chronological distribution at which a signal arrives at each node is calculated through use of the static timing analysis technique.

Preferably, each node has a plurality of paths, and a current waveform is calculated in consideration of a case where each of the paths has a unique probability of change and signal arrival time.

Brief Description of the Drawings

FIG. 1 is a schematic illustration for describing the

concept of the present invention;

FIG. 2 is a block diagram showing a portion of a circuit used in a first embodiment of the present invention;

FIGS. 3A and 3B are graphs showing waveforms of signals arriving at the respective nodes of the cell shown in FIG. 2;

FIG. 4 is a block diagram showing the processing of a frequency characteristic calculation block according to a first embodiment of the present invention;

FIGS. 5A to 5D are illustrations for describing a processing image according to the first embodiment of the present invention;

FIG. 6 is a flowchart of processing of a current waveform calculation according to the first embodiment;

FIG. 7 is a block diagram showing the processing of a frequency characteristic calculation block according to a second embodiment of the present invention;

FIGS. 8A through 8D are illustrations for describing a processing image pertaining to the second embodiment;

FIG. 9 is a flowchart of processing of a current waveform calculation according to the second embodiment;

FIG. 10 is a block diagram showing a portion of a circuit used in a third embodiment of the present invention;

FIG. 11 is a graph showing signal waveforms of each path;

FIG. 12 is a block diagram showing a frequency characteristic calculation block according to a third

embodiment of the present invention;

FIGS. 13A through 13C are illustrations showing a processing pertaining image to the third embodiment;

FIG. 14 is a flowchart of current waveform calculation processing according to the third embodiment;

FIG. 15 is a flowchart for describing a known EMI analysis method; and

FIG. 16 is a flowchart for describing a method of analyzing EMI dynamic at gate-level.

Description of the preferred Embodiments

An electromagnetic interference analysis method according to preferred embodiments of the present invention will now be described by reference to the accompanying drawings. As shown in FIG. 1, an EMI analysis method according to the present invention is characterized in:

calculating the transition probability of a node from a netlist 1 and a transition probability 2, through use of a propagation probability method, and calculating a static delay 4 through use of a static delay analysis method, to thereby derive a calculated probability/delay 5 of a node;

estimating the waveform 6 of an electric current on the basis of the probability/delay 5 and information 3 concerning the waveform of an electric signal at the time of toggling, to thereby derive a current waveform estimation result 7; and

subjecting the current waveform estimation result 7 to

a fast Fourier transformation 8 (hereinafter called an "FFT"), thereby determining a frequency characteristic 9 of the waveform.

(First Embodiment)

A method of analyzing electromagnetic interference according to a first embodiment of the present invention will be described hereinbelow. As can be seen from a schematic diagram shown in FIG. 1, under an EMI analysis method according to the present embodiment,

the quantity of electromagnetic interference developing in an LSI is to be analyzed on the basis of a transient probability and static delay propagation data, provided that a waveform shown in FIG. 3A appears in a node A of a flip-flop (FF) cell and a waveform shown in FIG. 3B appears in a node B of the FF cell (where FIG. 3B is an enlarged view of about 1.5 cycles of the signal designated by braces in FIG. 3A) when a clock signal CLK is input to a circuit shown in FIG. 2. Here, the transition probability of a node is calculated from a previously-prepared netlist 1 and a transition probability 2. Further, a static delay 4 in a current estimation waveform per change is calculated. The amplitude of a current waveform is corrected in consideration of information 3 concerning the waveform of an electric current arising at the time of a predetermined toggling operation. Provided that the corrected current waveform arises at a time at which a signal

arrives at the respective node, the current waveforms which appear at all nodes during a period of time corresponding to one cycle are added (the current waveform estimation processing 6). The current waveform estimation result 7 determined through addition is subjected to the FFT processing 8, thereby determining the frequency characteristic 9 of EMI components of a circuit to be analyzed.

FIG. 4 is a block diagram for describing the overall flow of processing of the EMI analysis method according to the present embodiment. FIGS. 5A through 5D are illustrations showing the principle underlying the processing. In a netlist 401, a circuit which is an object of EMI analysis is represented as circuit data. Delay information 405 concerning each node is formed from the netlist 401 through static delay calculation 403 (see FIG. 5A). Transition probability information 406 concerning each node is formed from the netlist 401 and input transition probability 402, through propagation probability 404 (see FIG. 5B). In consideration of a triangular waveform whose area corresponds to the quantity of electric current derived by means of multiplying current waveform information by probability information, an average current waveform 409 is formed by average current waveform calculation means 408 from element current waveform information 407 concerning each node (see FIG. 5C) and the delay information 405. The thus-determined average current waveform 409 is taken as

average current waveform information (see FIG. 5D). The average current waveform information is subjected to FFT processing 410, thereby deriving frequency characteristic information 411.

FIG. 6 shows a flowchart of processing of the average current waveform calculation means 408. The average current waveform calculation means 408 reads element current waveform information from a table (step 1250) and performs a current waveform calculation loop (step 1251). The base of a triangular waveform of an instance to be processed is extracted from an output slew (step 1252). The area of the triangular waveform is taken as being derived by means of multiplying $W \times \frac{h}{2}$ by transition probability per cycle, and I is taken as the value of the area of the triangular waveform. The height "h" of the triangular waveform is calculated from transition probability per $\frac{2 \times I}{W \times 1}$ cycle (step 1253), wherein "I" denotes the quantity of electric current flowing in a cell of an event which is an object of processing. This processing corresponds to processing performed by a triangular waveform shaping section. Until variable "x" changes from 0 to W/2, h(c, i) expressed (by Eq.5) is added to I(t+x) and I(t-x). Further, Δt is added to variable "x" (steps 1254 and 1255). Here, I(t+x) denotes total electric current flowing through all the cells at time

t+x, and I(t-x) denotes total electric current flowing through all the cells at time t-x.

The frequency characteristic of a circuit to be analyzed can be determined in the manner as mentioned previously, and a designer can analyze EMI which would arise in a circuit of interest.

According to the EMI analysis method, a current waveform is modeled through an averaging operation, on the basis of static delay information and propagation probability information. The thus-obtained model is subjected to FFT processing, thereby analyzing EMI of a circuit. The EMI analysis method can analyze EMI components within a shorter period of time than can a known gate-level dynamic analysis method.

In a case where performance of EMI analysis for each path of a circuit is desired, static delay information concerning each path is given.

In the present embodiment, electric currents of all nodes in a circuit to be analyzed are added. However, so long as the number of nodes whose electric currents are to be added is controlled in accordance with the magnitude of an electric current or the frequency of probability, processing time can be shortened further.

(Second Embodiment)

Next will be described an EMI analysis method according

to a second embodiment of the present invention. As represented by a flowchart shown in FIG. 7, the present EMI analysis method is characterized in employing random current waveform estimation means 708 in lieu of the average current waveform calculation means 408 employed in the first embodiment, and utilizing random current waveform information in lieu of the average current waveform information. In other respects, the EMI analysis method according to the present embodiment is identical in configuration with that described in connection with the first embodiment.

FIG. 7 a block diagram for describing the overall flow of processing of the EMI analysis method according to the present embodiment. FIGS. 8A through 8D are illustrations showing the principle underlying the processing. In a netlist 701, a circuit which is an object of EMI analysis is represented as circuit data. Delay information 705 concerning each node is formed from the netlist 701 through static delay calculation 703 (see FIG. 8A). Transition probability information 706 concerning each node is formed from the netlist 701 and input transition probability 702, through propagation probability 704 (see FIG. 8B). On the basis of element current waveform information 707 concerning each node (FIG. 8C) and operating frequency information 712, random waveform estimation means 708 produces random current waveform information 709 (see FIG. 8D) within a plurality of predetermined cycles. The thus-

produced random current waveform information 709 is subjected to FFT processing 710, thereby deriving frequency characteristic information 711.

FIG. 9 shows a flowchart of processing of the random current waveform estimation means 708. The average current waveform estimation means 708 reads element current waveform information from a table (step 1280) and performs a current waveform calculation loop (step 1281). The average current waveform estimation means 708 performs loop processing until valuable "y" changes from 1 to the value of a frequency. (step 1282). The following processing is iterated until calculation of a current waveform is completed. A determination is made as to whether or not a random number is smaller than the value of probability (step 1283). If a random number is smaller, the base of a triangular waveform of an instance to be processed is extracted from an output slew (step 1284). At this time, the area of the triangular waveform is defined as $W \times \frac{h}{2}$, and I is the value of the area of the triangular waveform. The height "h" of the triangular waveform is calculated by $2 \times \frac{I}{W}$ (step 1285), wherein "I" denotes the quantity of electric current flowing in a cell of an event which is an object of processing. This processing corresponds to processing performed by a triangular waveform shaping section. Until

variable "x" changes from 0 to W/2, h(c, i) expressed (by Eq.5) is added to I(t+x) and I(t-x). Further, Δt is added to variable "x" (steps 1286 and 1287). Here, I(t+x) denotes total electric current flowing through all the cells at time t+x, and I(t-x) denotes total electric current flowing through all the cells at time t-x.

The frequency characteristic of a circuit to be analyzed can be determined in the manner as mentioned previously, and a designer can analyze EMI which would arise in a circuit of interest.

According to the EMI analysis method, a current waveform is modeled through a random current waveform operation, on the basis of static delay information and propagation probability information. The thus-obtained model is subjected to FFT processing, thereby analyzing EMI of a circuit. The EMI analysis method can analyze EMI components with high accuracy within a shorter period of time than a known gate-level dynamic analysis method.

In a case where performance of EMI analysis for each path of a circuit is desired, static delay information concerning each path is given.

In the present embodiment, electric currents information of all nodes in a circuit to be analyzed are added. However, so long as the number of nodes whose electric currents are to be added is controlled in accordance with the magnitude of an

electric current or the frequency of probability, processing time can be shortened further.

(Third Embodiment)

An EMI analysis method according to a third embodiment of the present invention will now be described. In the previously-described first and second embodiments, delay information and probability information are prepared separately. Information is derived by means of multiplying waveform information which is obtained as element current waveform information, by probability information. The thus-obtained information is added to a delay time of each node. In contrast, in the present embodiment, delay propagation probability information is formed from delay propagation probability information. Delay/transition probability is calculated from the delay propagation probability information, and element waveform information is added to the thus-calculated delay/transition probability.

In this way, more realistic current waveform information is calculated, and the result of current waveform calculation is subjected to FFT processing, thereby determining the frequency characteristic of an EMI component of a circuit to be analyzed. Thus, EMI of the circuit is analyzed. As can be seen from an enlarged view shown in FIG. 10, the present embodiment is directed particularly a case where a plurality of paths are provided in a composite cell. FIG. 11 shows delay

transition information concerning propagation of a signal in each of the paths of the composite cell shown in FIG. 10. FIG. 11 shows delay transition probability information as one example. As can be seen from FIG. 11, there is obtained node information concerning a plurality of paths, and mean current waveform information is formed from the node information.

FIG. 12 is a block diagram for describing the overall flow of processing of the EMI analysis method according to the present embodiment. FIGS. 13A through 13C are illustrations showing the principle underlying the processing. FIG. 14 is a flowchart of average current waveform calculation means used in the processing. In a netlist 901, a circuit which is an object of EMI analysis is represented as circuit data. Delay/transition probability 906 of each node is calculated from the netlist 901 and input transition probability 902, on the basis of delay/propagation probability 904 (see FIG. 13A). Mean current waveform estimation means 908 produces mean current waveform information 909 (see FIG. 13C), in consideration of a triangular waveform whose area is determined by the quantity of electric current, such that the delay/transition probability 906 is multiplied by element current waveform information 907 (see FIG. 13B). The thus-formed mean current waveform information 909 is subjected to FFT processing 910 within a time domain which is determined on the basis of operating frequency information 912, thereby

obtaining frequency characteristic information 911.

FIG. 14 shows a flowchart of processing of the average current waveform calculation means. The average current waveform calculation means reads element current waveform information from a table (step 1310) and performs a current waveform calculation loop (step 1311). The following processing is iterated until calculation of a current waveform is completed. The delay/transition probability 906 calculated from delay information and transition probability information is multiplied by element current waveform information 907 (see FIG. 13B) (step 1312). In consideration of a triangular waveform whose area is determined by the quantity of electric current, average electric current waveform estimation means 908 adds the result of multiplication as mean current, thereby deriving average current waveform information 909. The average current waveform information 909 is subjected to FFT processing 910, thereby determining frequency characteristic information 911.

The frequency characteristic of a circuit to be analyzed can be determined in the manner as mentioned previously, and a designer can analyze EMI, which would arise in a circuit of interest.

According to the EMI analysis method, delay propagation probability information is formed from static delay information and propagation probability information, and average current waveform information is formed from the delay propagation probability information. The thus-obtained average current waveform information is subjected to FFT processing, thereby enabling highly-accurate EMI analysis. The EMI analysis method can analyze EMI components within a shorter period of time than can a known gate-level dynamic analysis method.

In addition to a distribution taking into consideration a path, a temperature/process/voltage distribution may be conceived as the delay/transition probability information shown in FIG. 13A.

In the foregoing embodiments, FFT processing has been used for analyzing a frequency. However, the present invention is not limited to FFT processing. Needless to say, another processing method, such as ordinary Fourier transformation, may alternatively be employed.

The present invention can materialize evaluation of EMI developing in an LST through a simulation, by means of

highly-accurately analyzing through static processing, variation in power-supply current which may be said to primarily account for EMI. Further, in contrast with dynamic analysis of EMI which is embodied by a gate-level simulation or a like simulation, the present EMI analysis method can prevent an increase in processing time.

What is claimed is:

1. A method of analyzing electromagnetic interference developing in an LSI, comprising:

a correction step of correcting the amplitude of a current estimation waveform in each node which has been previously prepared for each change in each node, in accordance with the probability of variation in each node;

an addition step of adding current waveforms of all nodes together within a period of time corresponding to one cycle, provided that the thus-corrected current waveform appears at a time a signal arrives at each node; and

a frequency analysis step of analyzing the frequency of the current waveform calculated in the addition step.

2. The method of analyzing electromagnetic interference developing in an LSI according to claim 1, wherein the correction step includes a step of correcting the amplitude of a current estimation waveform, which has been prepared for each change in each node, in accordance with the probability of variation in each node and a distribution with respect to time.

3. The method of analyzing electromagnetic interference developing in an LSI according to claim 1, wherein each node has a plurality of signal transmission paths (hereinafter referred to simply as "paths"), and each of the current waveforms is calculated in consideration of a case where each

of the paths has a unique probability of change and signal arrival time.

4. The method of analyzing electromagnetic interference developing in an LSI according to claim 2, wherein each node has a plurality of paths, and each of the current waveform is calculated in consideration of a case where each of the paths has a unique probability of change and signal arrival time.

5.A method of analyzing electromagnetic interference developing in an LSI, the method comprising:

a waveform formation step of forming a current estimation waveform which has been prepared for each change in each node, as if the waveform randomly arises within a plurality of predetermined cycles, in accordance with the probability of change in each node and a time at which a signal arrives at each node;

adding the thus-prepared current estimation waveforms of all nodes, to thereby derive a current waveform; and

analyzing the frequency of the current waveform, thereby determining a noise characteristic of EMI.

6. The method of analyzing electromagnetic interference developing in an LSI according to claim 5, wherein each node has a plurality of paths, and a current waveform is calculated in consideration of a case where each of the paths has a unique probability of change and signal arrival time.

7. A method of analyzing electromagnetic interference

developing in an LSI, the method comprising:

a waveform formation step of forming a current estimation waveform which has been prepared for each change in each node, as if the waveform randomly arises within a plurality of predetermined cycles, in accordance with the probability of change in each node and a distribution probability of time;

adding the thus-prepared current estimation waveforms of all nodes, to thereby derive a current waveform; and

analyzing the frequency of the current waveform, thereby determining a noise characteristic of EMI.

8. The method of analyzing electromagnetic interference developing in an LSI according to claim 7, wherein each node has a plurality of paths, and a current waveform is calculated in consideration of a case where each of the paths has a unique probability of change and signal arrival time.

Abstract

In contrast with a known dynamic gate-level simulation method, a method of analyzing electromagnetic interference (an EMI analysis method) according to the present invention enables estimation of EMI noise, by means of calculating signal propagation of each node through use of the signal propagation probability technique, and calculating variation time of each node through use of "the Static timing analysis technique". In short, the present invention is characterized in calculating a frequency characteristic from the relationship between toggle probability of each node and delay in each node.

Fig.1

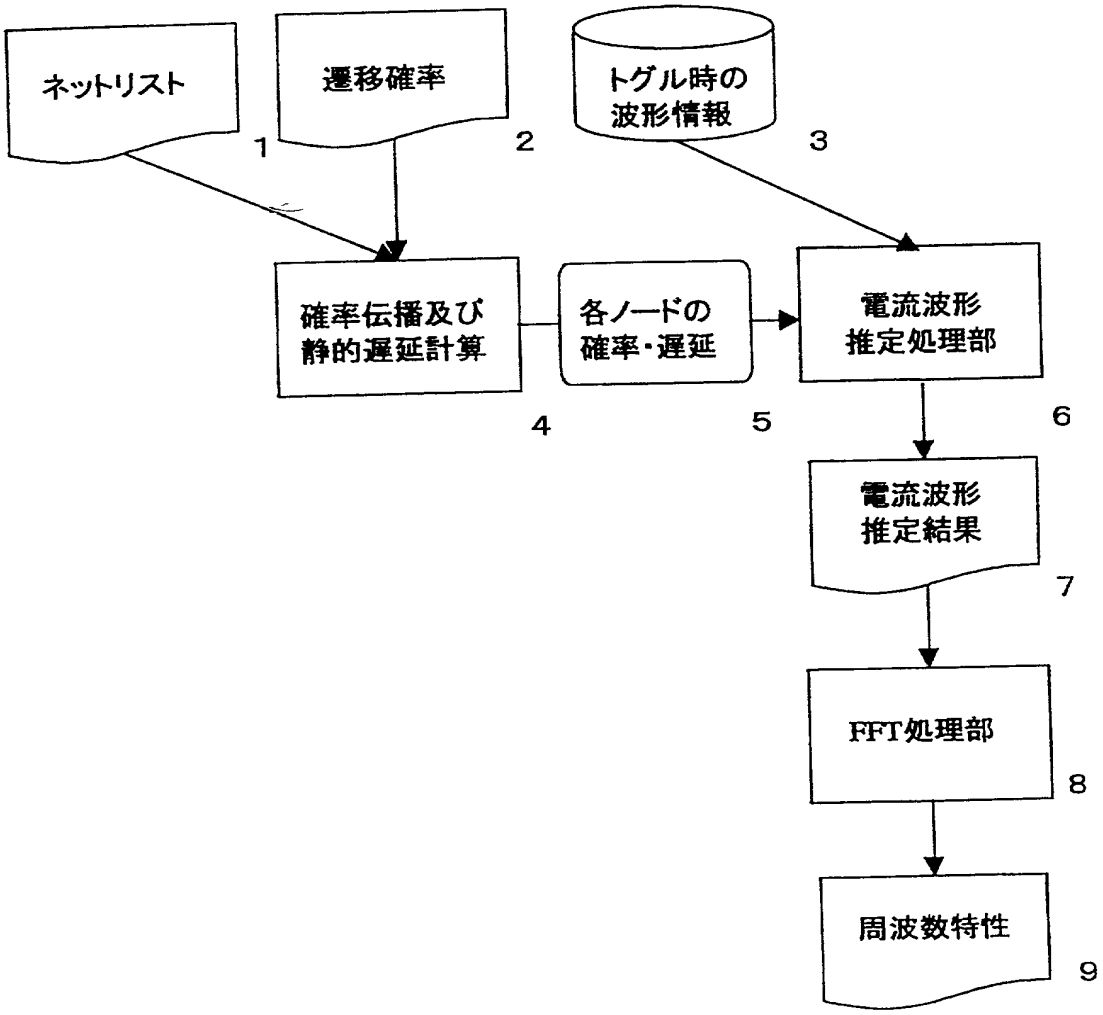


Fig.2

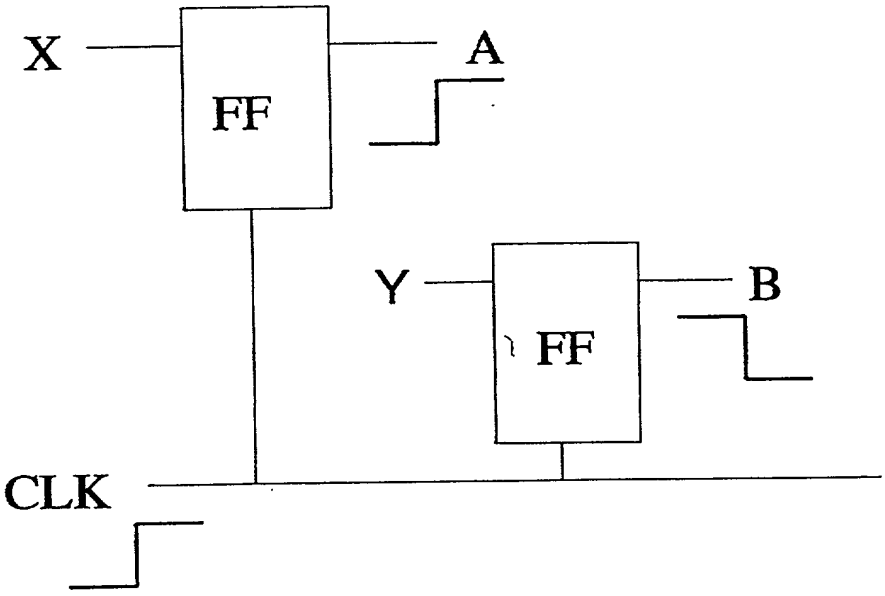


Fig.3A

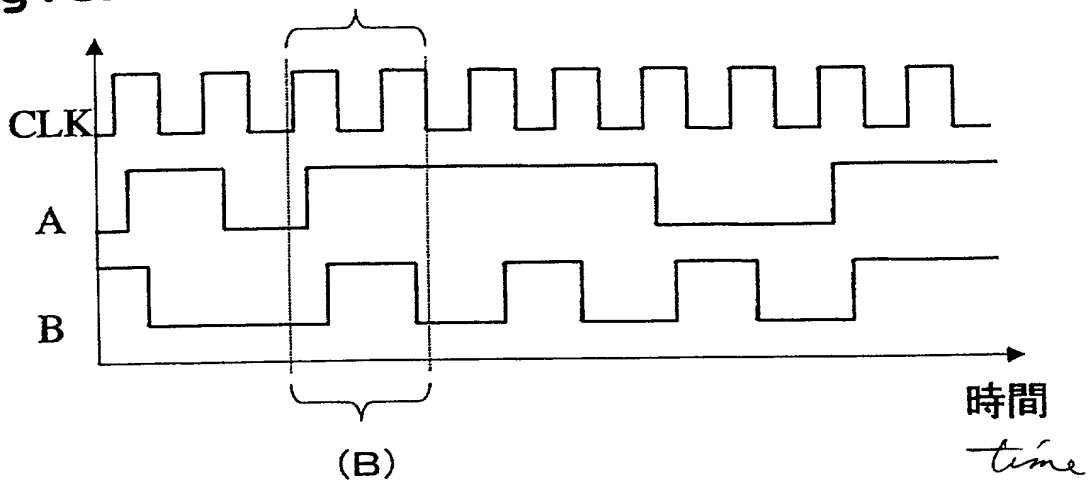


Fig.3B

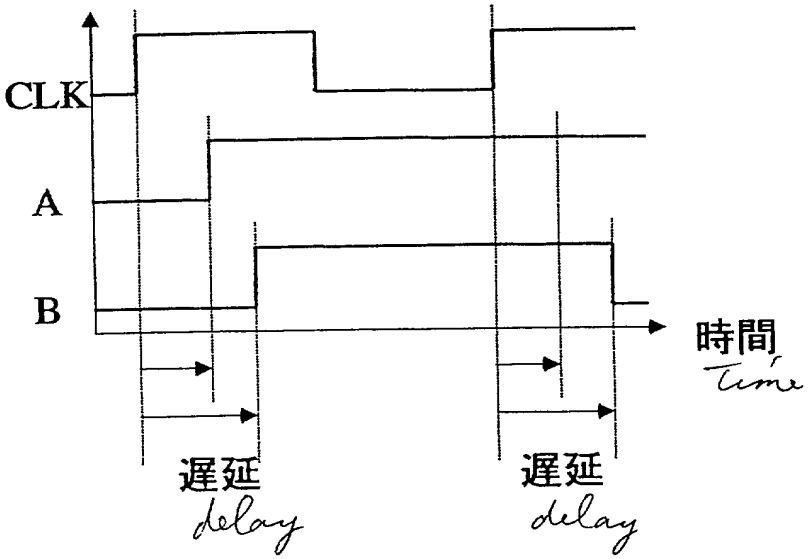


Fig.4

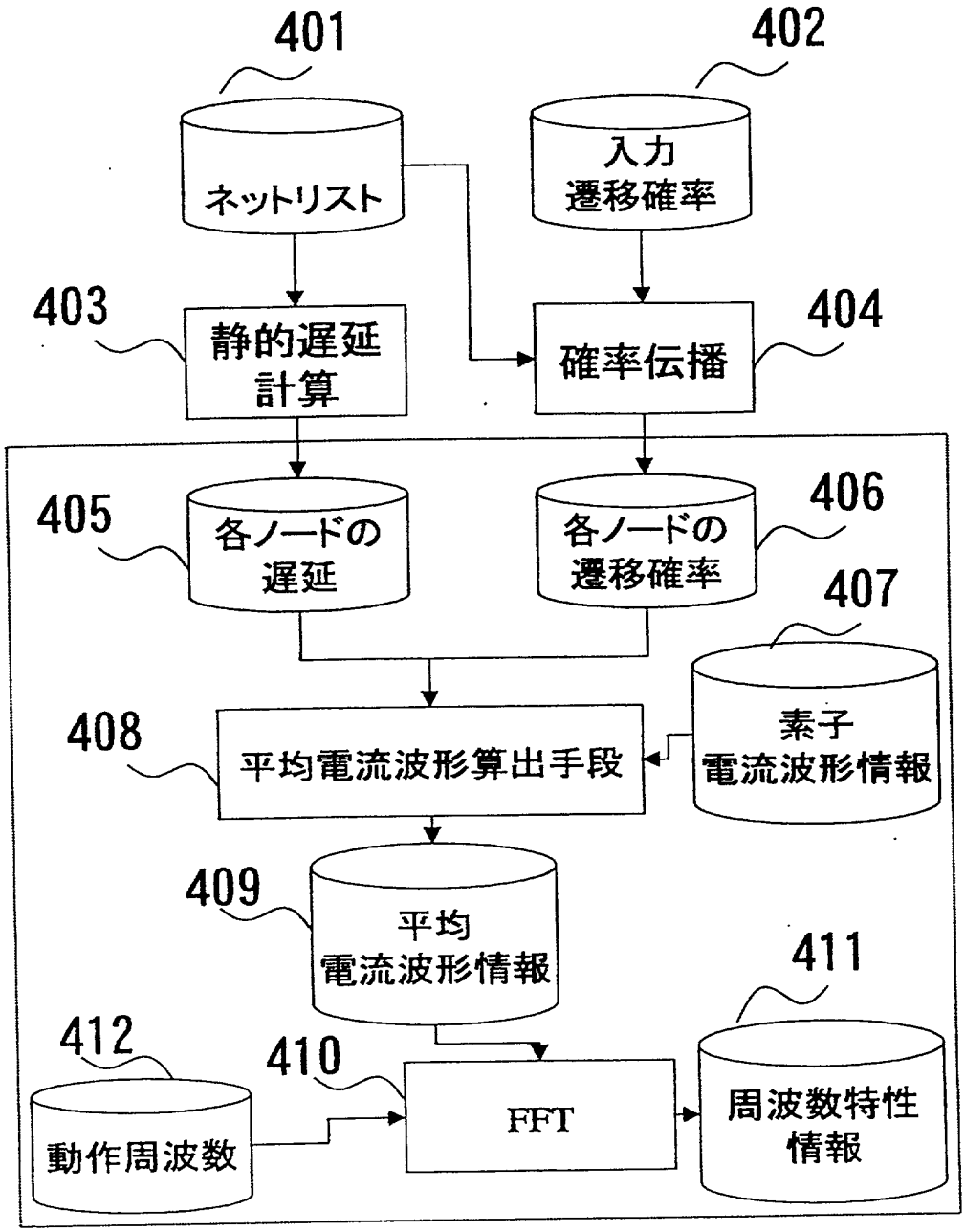


Fig.5A

(a)遅延情報

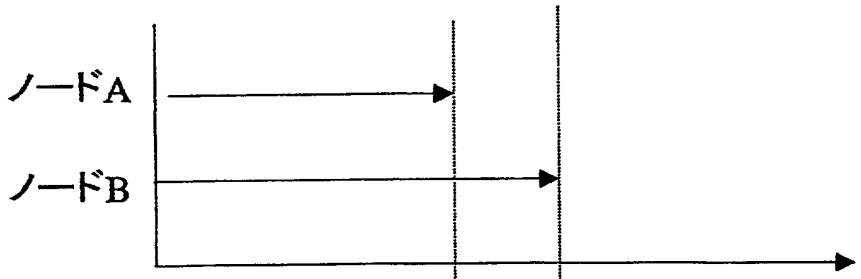


Fig.5B　確率情報

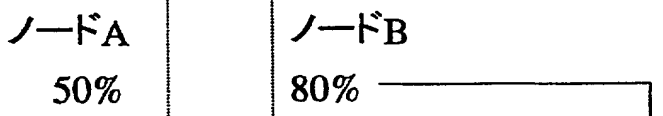


Fig.5C　素子電流波形情報

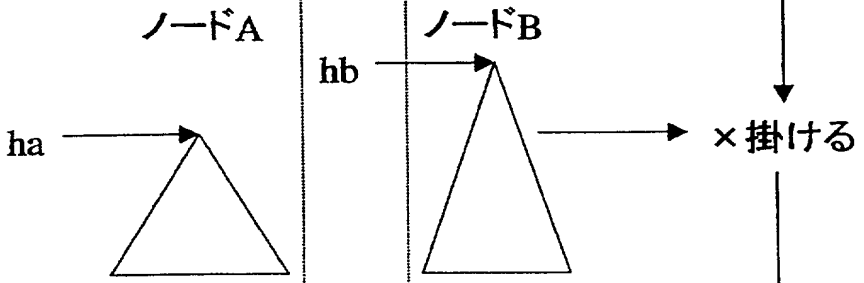


Fig.5D 平均電流波形情報

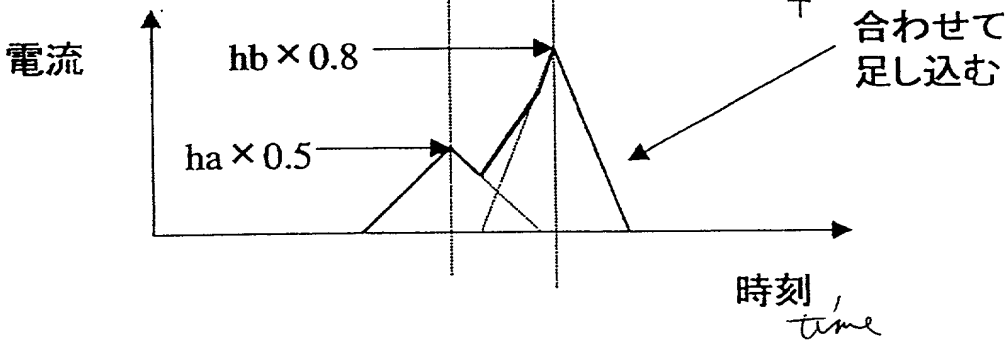


Fig.6

平均電流波形算出手段処理フロー図

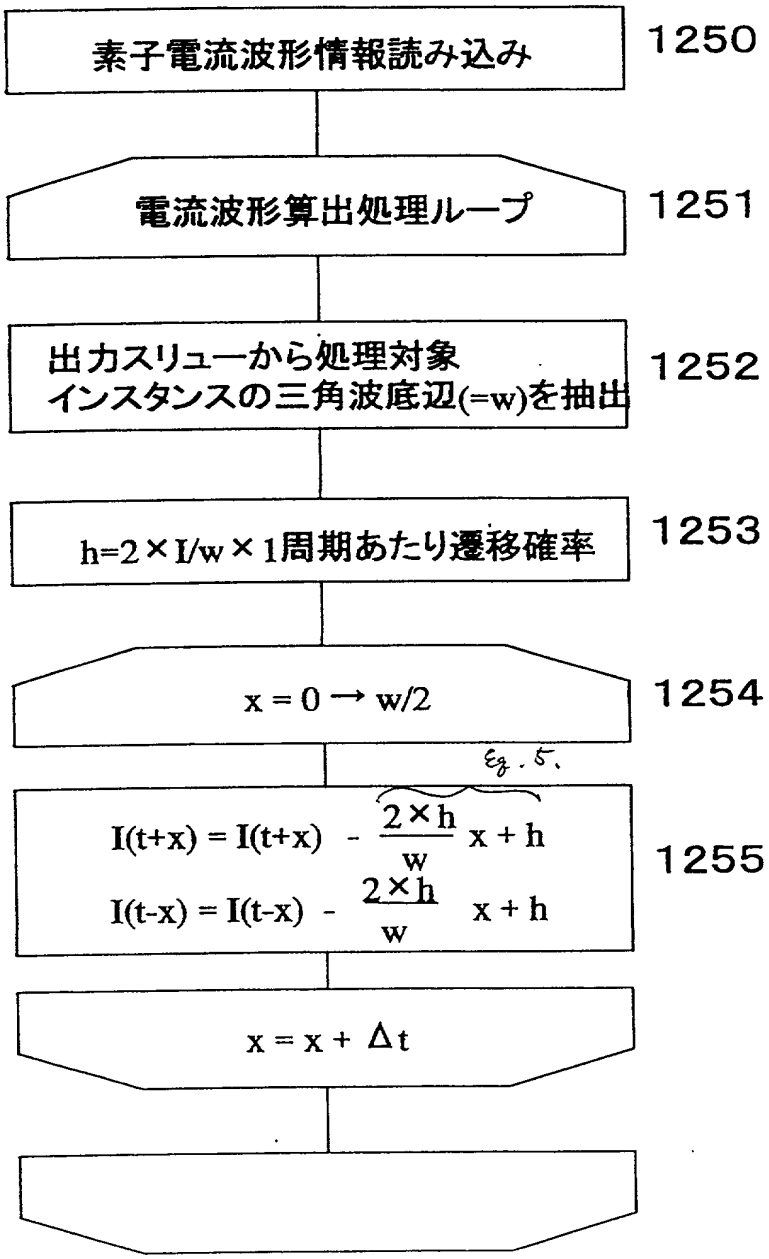


Fig.7

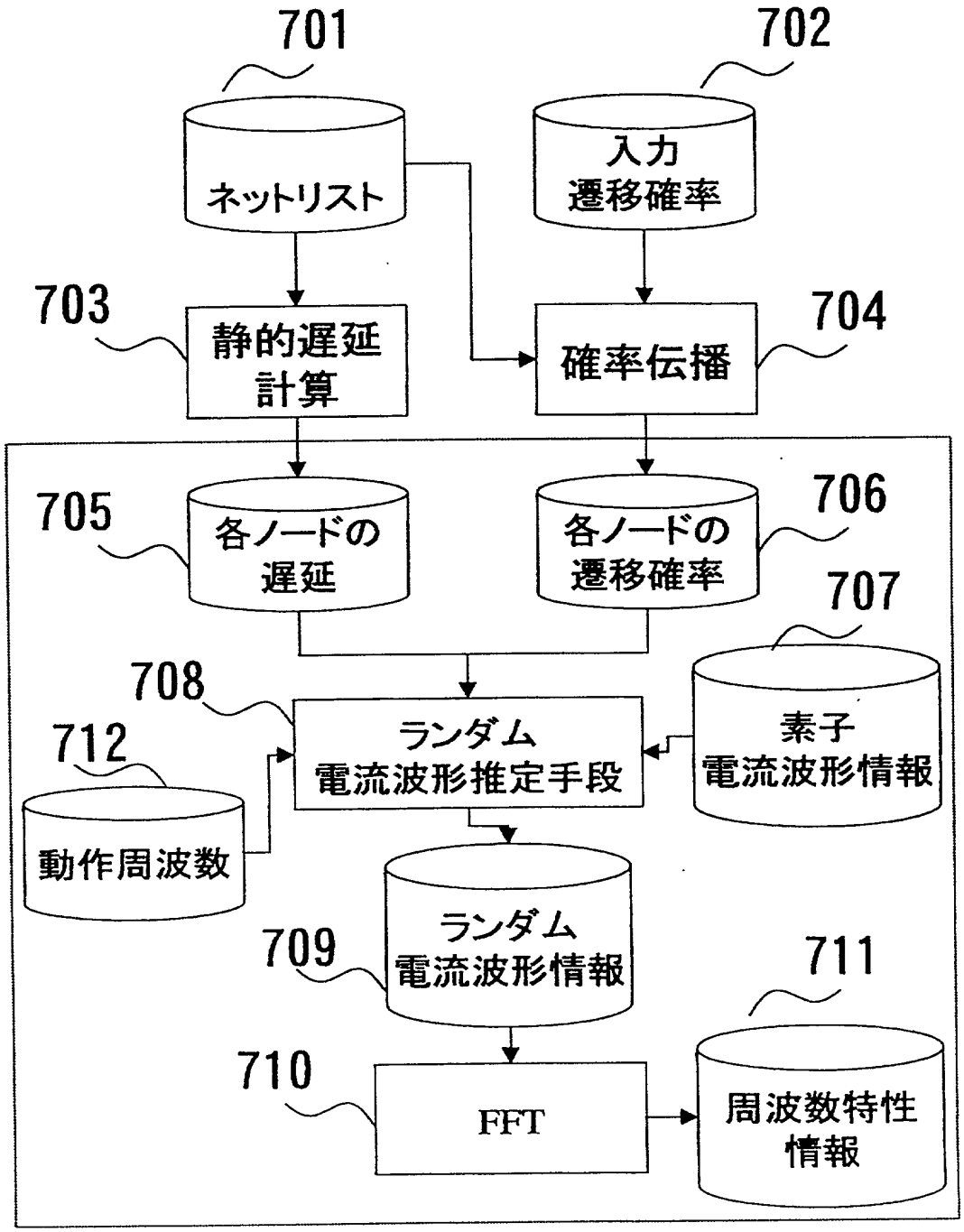

701
ネットリスト
702
入力
遷移確率
703
静的遅延
計算
704
確率伝播
705
各ノードの
遅延
706
各ノードの
遷移確率
707
素子
電流波形情報
708
ランダム
電流波形推定手段
712
動作周波数
709
ランダム
電流波形情報
711
710
FFT
周波数特性
情報

Fig.8A遅延情報

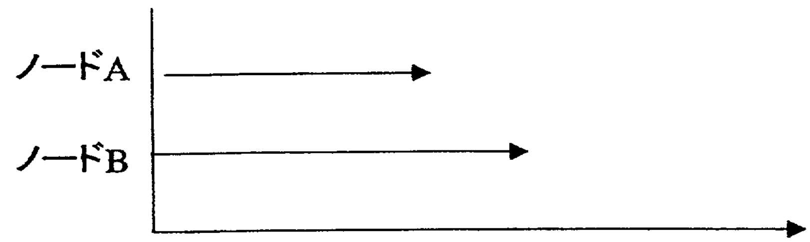


Fig.8B 確率情報

ノードA	ノードB
50%	80%

Fig.8C 素子電流波形情報

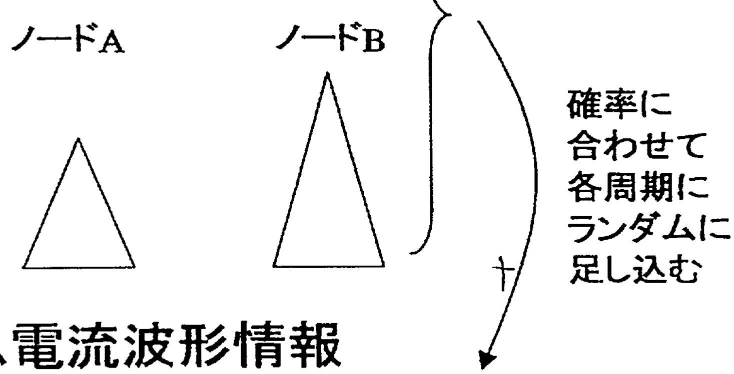


Fig.8D ランダム電流波形情報

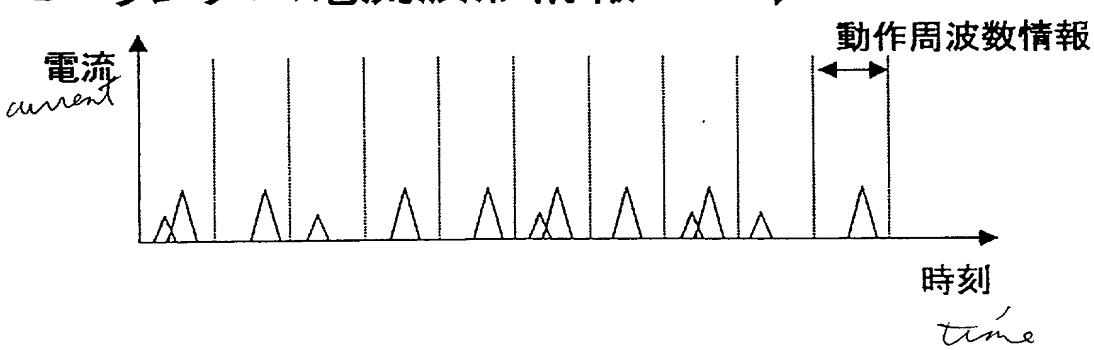


Fig.9

ランダム電流波形算出手段処理フロー図

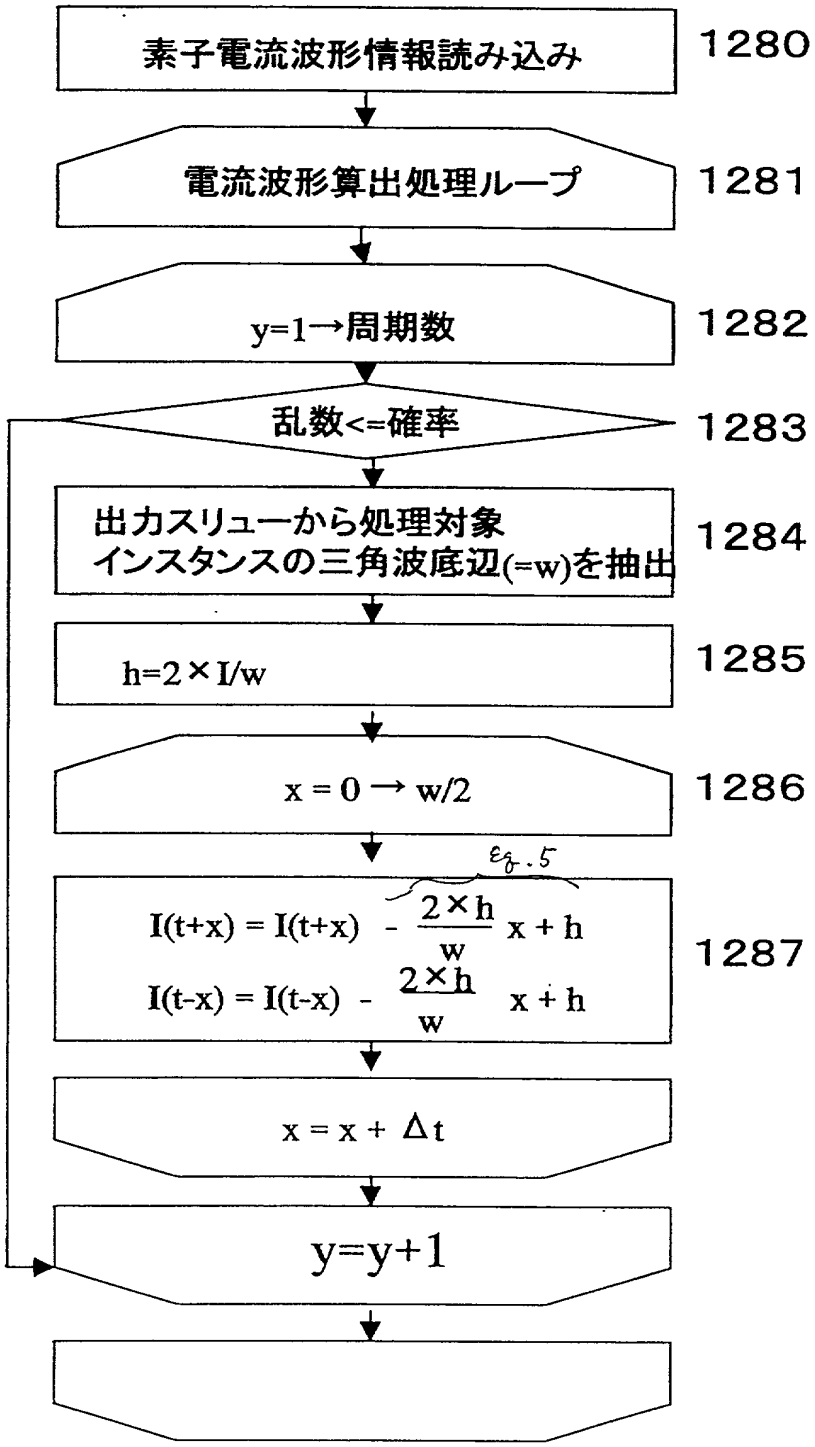


Fig.10

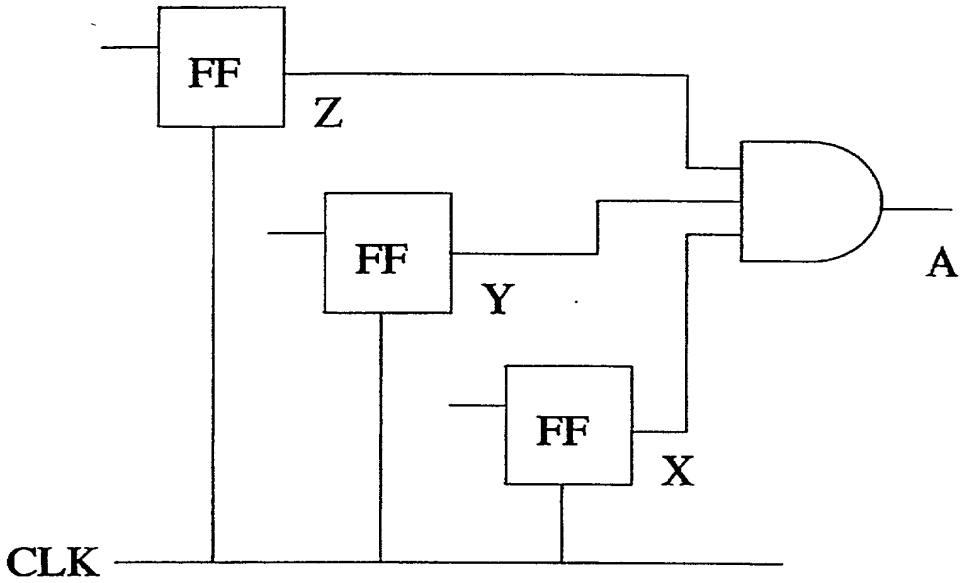
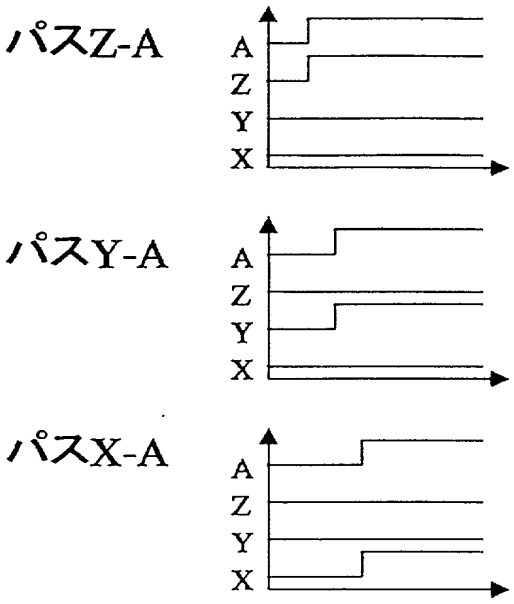


Fig.11



複数パス毎の遅延・遷移確率情報を盛り込む。

Fig.12

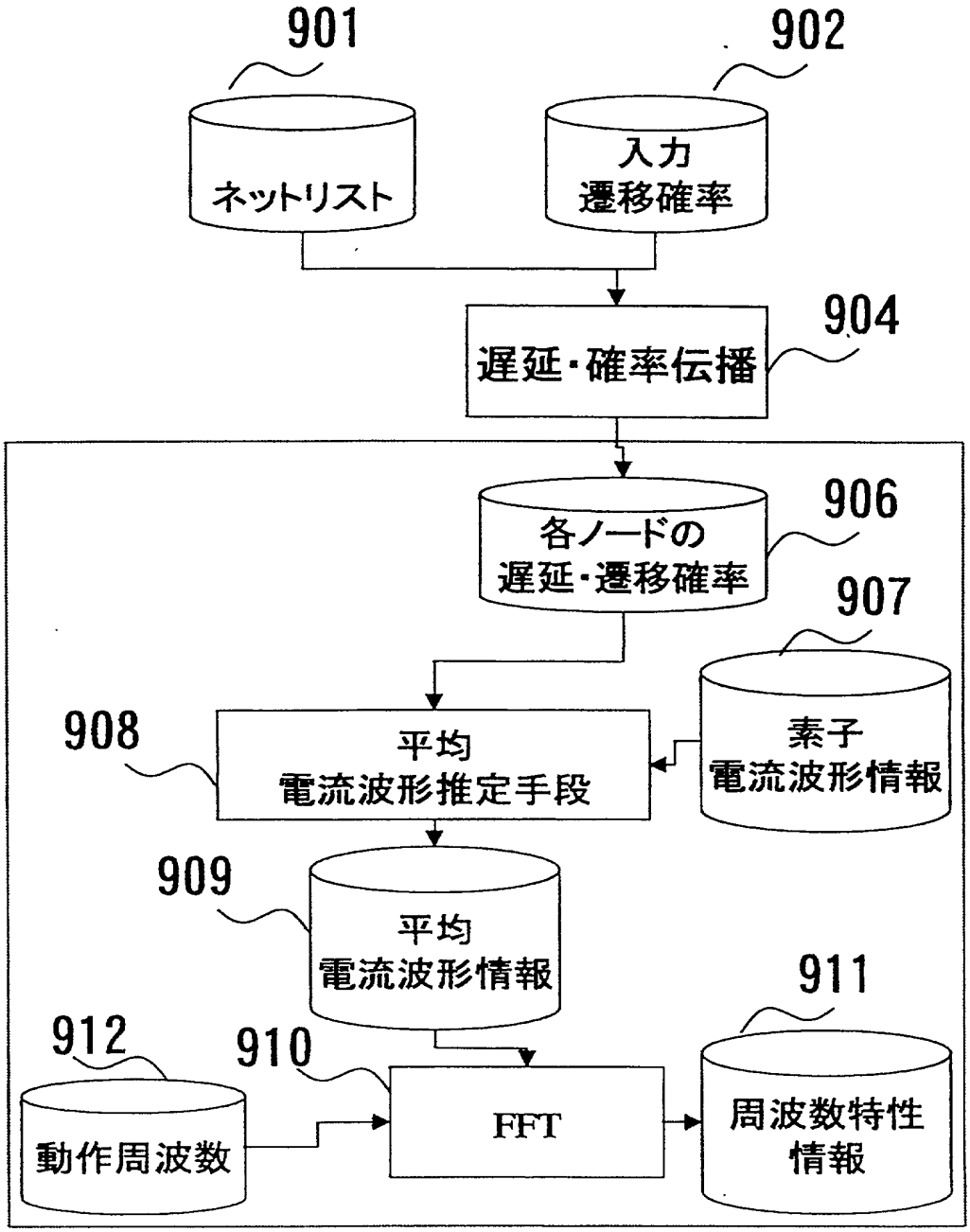

901
902
ネットリスト
入力
遷移確率
904
遅延・確率伝播
906
各ノードの
遅延・遷移確率
907
908
平均
電流波形推定手段
素子
電流波形情報
909
平均
電流波形情報
911
912
910
動作周波数
FFT
周波数特性
情報

Fig.13A 遅延・遷移確率情報

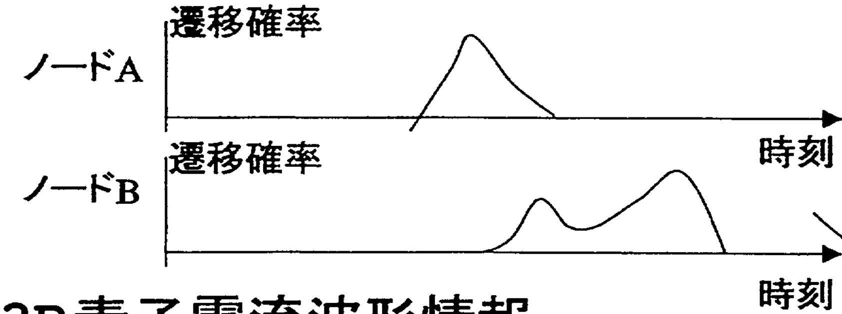


Fig.13B 素子電流波形情報

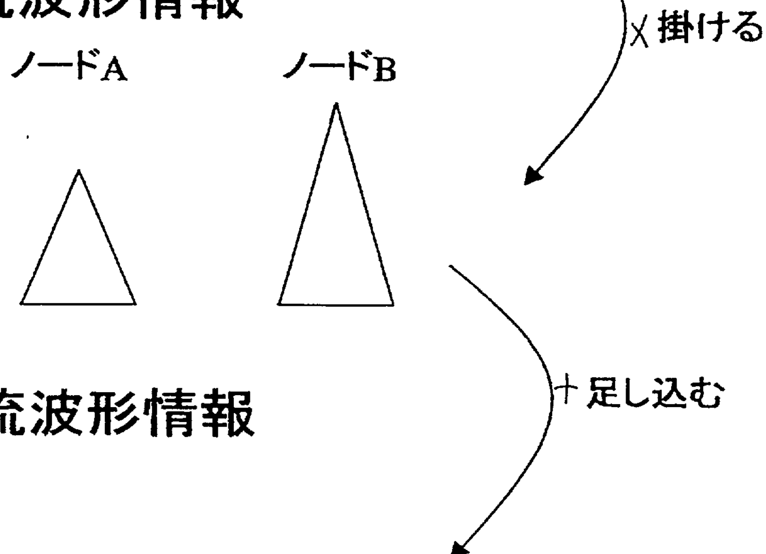


Fig.13C 平均電流波形情報

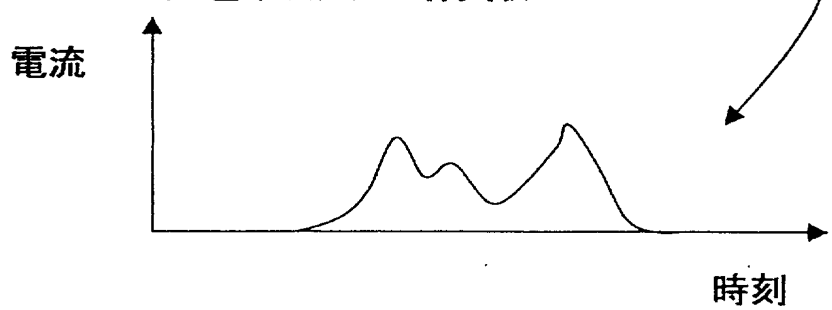


Fig.14

平均電流波形算出手段処理フロー図

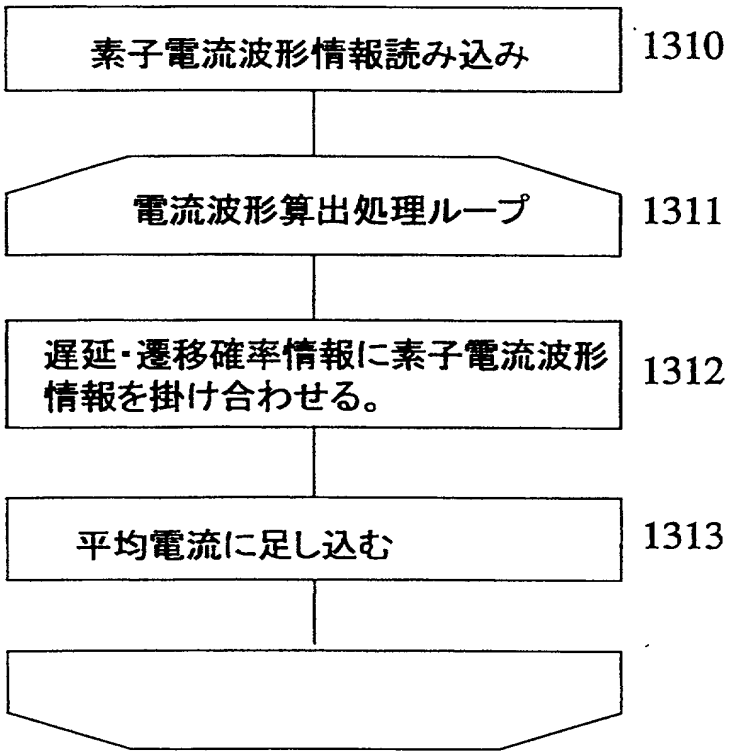


Fig.15

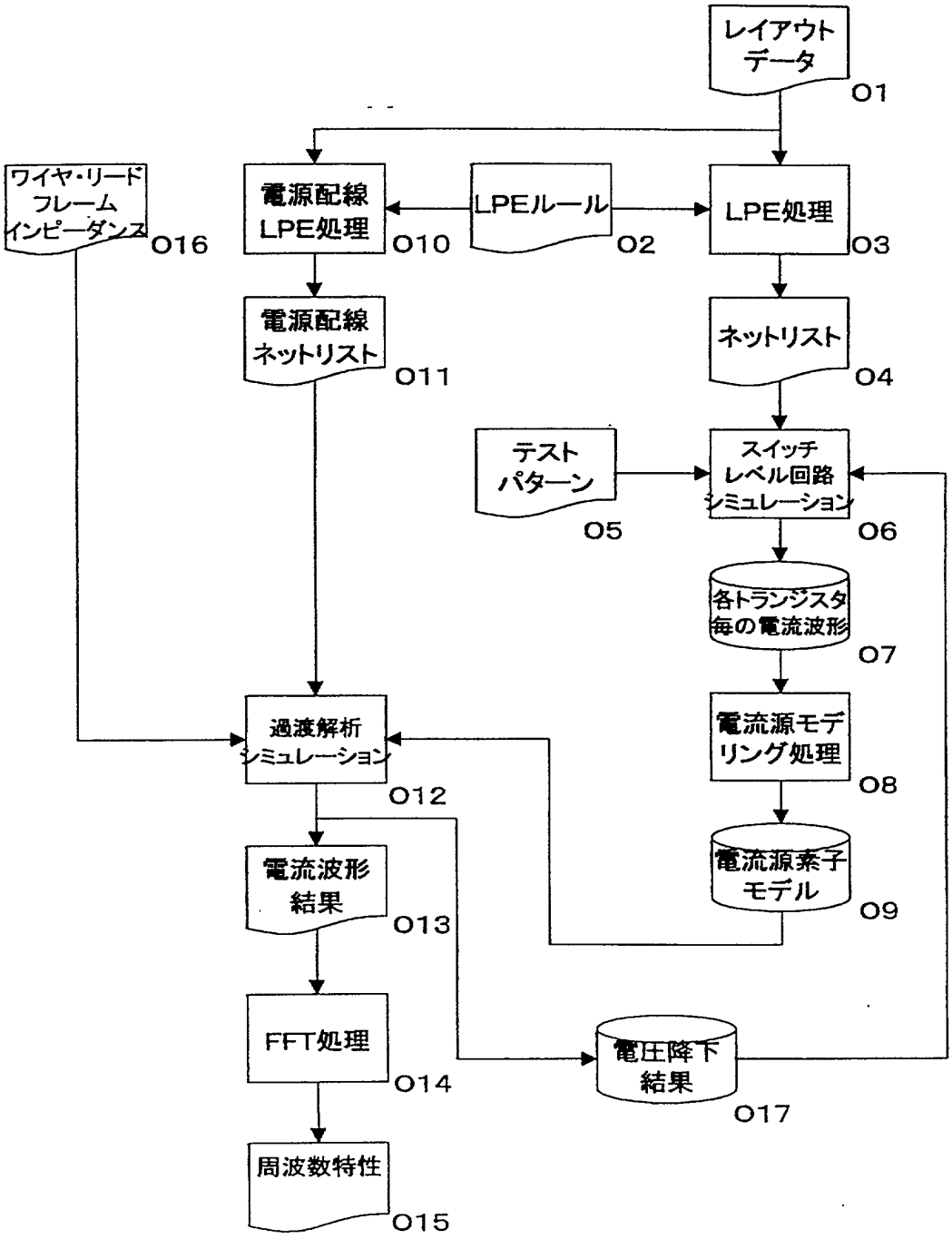
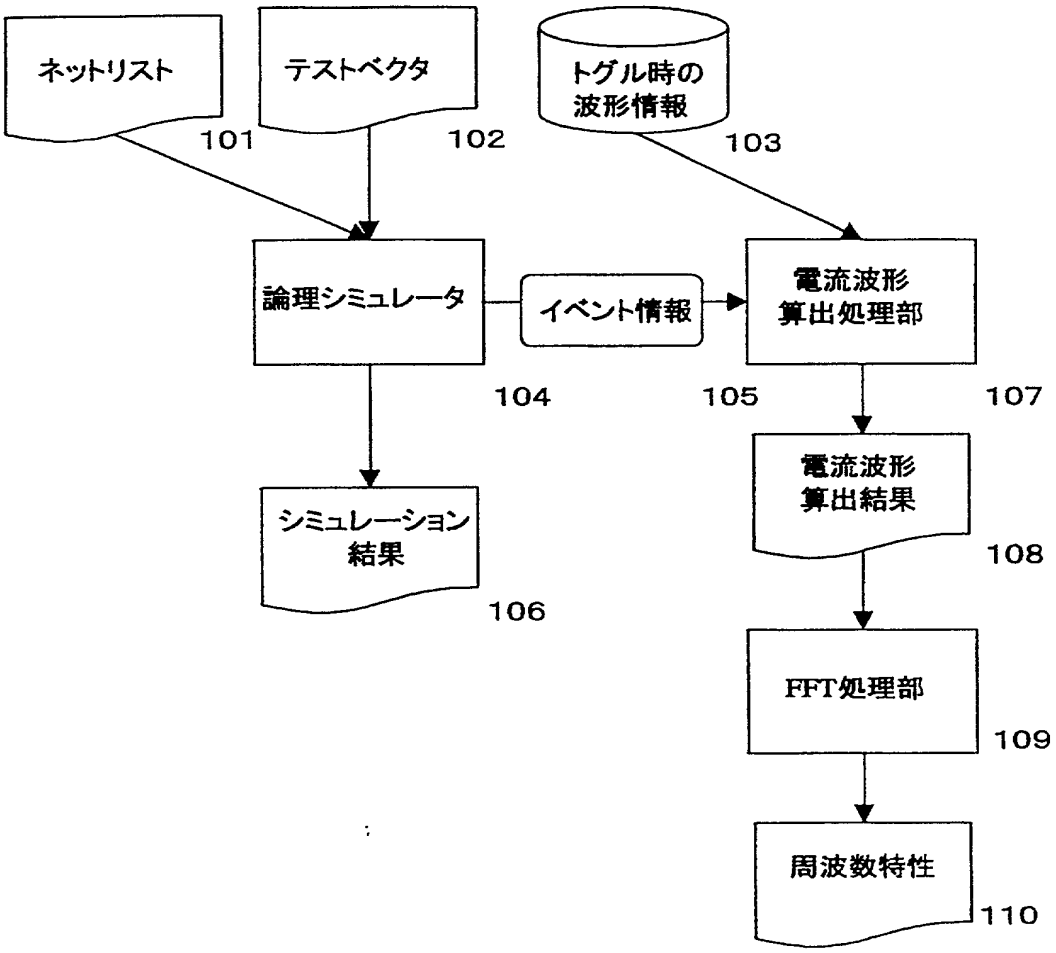

レイアウトデータ
O1
ワイヤ・リードフレームインピーダンス
O16
電源配線LPE処理
O10
LPEルール
O2
LPE処理
O3
電源配線ネットリスト
O11
ネットリスト
O4
テストパターン
O5
スイッチレベル回路シミュレーション
O6
各トランジスタ毎の電流波形
O7
過渡解析シミュレーション
O12
電流源モデリング処理
O8
電流源素子モデル
O9
電流波形結果
O13
FFT処理
O14
電圧降下結果
O17
周波数特性
O15

Fig.16



[DESIGNATION OF DOCUMENT] DRAWINGS

[FIG. 1]

1 NETLIST

2 TRANSITION PROBABILITY

3 WAVEFORM INFORMATION FORMED AT THE TIME OF TOGGLING

4 PROPAGATION PROBABILITY AND CALCULATION OF STATIC DELAY

5 PROBABILITY AND DELAY OF RESPECTIVE NODE

6 CURRENT WAVEFORM ESTIMATION SECTION

7 CURRENT WAVEFORM ESTIMATION RESULT

8 FFT PROCESSING SECTION

9 FREQUENCY CHARACTERISTIC

[FIG. 3A]

TIME

[FIG. 3B]

DELAY, DELAY, TIME

[FIG. 4]

401 NETLIST

402 INPUT TRANSITION PROBABILITY

403 STATIC DELAY CALCULATION

404 PROPAGATION PROBABILITY

405 DELAY OF RESPECTIVE NODE

406 TRANSITION PROBABILITY OF RESPECTIVE NODE

407 ELEMENT CURRENT WAVEFORM INFORMATION

408 AVERAGE CURRENT WAVEFORM CALCUALTION MEANS

409 AVERAGE CURRENT WAVEFORM INFORMATION

411 FREQUENCY CHARACTERISTIC INFORMATION

412 OPERATING FREQUENCY

[FIG. 5A]

DELAY INFORMATION

NODE A, NODE B

[FIG. 5B]

PROBABILITY INFORMATION

NODE A, NODE B

[FIG. 5C]

ELEMENT CURRENT WAVEFORM INFORMATION

NODE A, NODE B

MULTIPLIED BY

[FIG. 5D]

AVERAGE CURRENT WAVEFORM INFORMATION

CURRENT, TIME

ADD INFORMATION TO DELAY TIME

[FIG. 6]

FLOWCHART OF AVERAGE CURRENT WAVEFORM CALCULATION PROCESSING

1250 READ ELEMENT CURRENT WAVEFORM INFORMATION

1251 CURRENT WAVEFORM CALCULATION LOOP

1252 EXTRACT, FROM OUTPUT SLEW DATA, THE BASE OF TRIANGULAR WAVEFORM

(=w) OF AN INSTANCE TO BE PROCESSED

1253 TRANSITION PROBABILITY PER h=2 X I/2 X 1

[FIG. 7]

701 NETLIST

702 INPUT TRANSITION PROBABILITY

703 STATIC DELAY CALCULATION

704 PROPAGATION PROBABILITY

705 DELAY OF RESPECTIVE NODE

706 TRANSITION PROBABILITY OF RESPECTIVE NODE

707 ELEMENT CURRENT WAVEFORM INFORMATION

708 RANDOM CURRENT WAVEFORM CALCUALTION MEANS

709 RANDOM CURRENT WAVEFORM INFORMATION

711 FREQUENCY CHARACTERISTIC INFORMATION

712 OPERATING FREQUENCY

[FIG. 8A]

DELAY INFORMATION

NODE A, NODE B

[FIG. 8B]

PROBABILITY INFORMATION

NODE A, NODE B

[FIG. 8C]

ELEMENT CURRENT WAVEFORM INFORMATION

NODE A, NODE B

RANDOMLY ADD INFORMATION TO RESPECTIVE CYCLE IN ACCORDANCE WITH PROBABILITY

[FIG. 8D]

RANDOM CURRENT WAVEFORM INFORMATION

CURRENT, TIME

OPERATING FREQUENCY INFORMATION

[FIG. 9]

FLOWCHART OF RANDOM CURRENT WAVEFORM CALCULATION PROCESSING

1280 READ ELEMENT CURRENT WAVEFORM INFORMATION

1281 CURRENT WAVEFORM CALCULATION LOOP

1282 PERFORM LOOP PROCESSING UNTIL y=1 ASSUMES THE VALUE OF A FREQUENCY

1283 DETERMINE WHETHER OR NOT A RANDOM NUMBER IS SMALLER THAN THE VALUE OF PROBABILITY

1284 EXTRACT, FROM OUTPUT SLEW DATA, THE BASE OF TRIANGULAR WAVEFORM (=w) OF AN INSTANCE TO BE PROCESSED

[FIG. 11]

ADD DELAY AND TRANSITION PROBABILITY INFORMATION UNIQUE TO EACH OF PATHS TO DELAY TRANSITION PROBABILITY INFORMATION

delay transition probability information

[FIG. 12]

901 NETLIST

902 INPUT TRANSITION PROBABILITY

903 DELAY AND PROPAGATION PROBABILITY

906 DELAY AND TRANSITION PROBABILITY OF RESPECTIVE NODE

907 ELEMENT CURRENT WAVEFORM INFORMATION

908 AVERAGE CURRENT WAVEFORM ESTIMATION MEANS

909 AVERAGE CURRENT WAVEFORM INFORMATION

911 FREQUENCY CHARACTERISTIC INFORMATION

912 OPERATING FREQUENCY

[FIG. 13A]

DELAY/TRANSITION PROBABILITY INFORMATION

NODE A, NODE B

TRANSITION PROBABILITY

TIME

[FIG. 13B]

ELEMENT CURRENT WAVEFORM INFORMATION

NODE A, NODE B

MULTIPLY

[FIG. 13C]

AVERAGE CURRENT WAVEFORM INFORMATION

ADD

CURRENT, TIME

[FIG. 14]

FLOWCHART OF PROCESSING PERTAINING TO AVERAGE CURRENT WAVEFORM CALCULATION MEANS

1310 READ ELEMENT CURRENT WAVEFORM INFORMATION

1311 CURRENT WAVEFORM CALCULATION LOOP

1312 MULTIPLY DELAY/TRANSITION PROBABILITY INFORMATION BY CURRENT WAVEFORM INFORMATION

1313 ADD RESULTANT INFORMATION TO AVERAGE CURRENT

[FIG. 15]

01 LAYOUT DATA

02 LPE RULE

03 LPE PROCESSING

04 NETLIST

05 TEST PATTERN

06 SWITCH-SCALE CIRCIT SIMULATION

07 CURRENT WAVEFORM OF RESPECTIVE TRANSISTOR

08 MODELING OF CURRENT SOURCE

09 MODELING OF CURRENT-SOURCE ELEMENT

010 POWER LINE LPE PROCESSING

011 POWER LINE NETLIST

012 TRANSITION ANALYSIS SIMULATION

013 CURRENT WAVEFORM RESULT

014 FFT PROCESSING

015 FREQUENCY CHARACTERISTIC

016 WIRE/LEADFRAME IMPEDANCE

017 VOLTAGE DROP RESULT

[FIG. 16]

101 NETLIST

102 TEST VECTOR

103 WAVEFORM INFORMATION FORMED AT THE TIME OF TOGGLING

104 LOGIC SIMULATOR

105 EVENT INFORMATION

106 SIMULATION ERSULT

107 CURRENT WAVEFORM CALCULATION SECTION

108 CURRENT WAVEFORM CALCULATION RESULT

109 FFT PROCESSING

110 FREQUENCY CHARACTERISTIC

Attorney's Docket No. 32809

COMBINED DECLARATION AND POWER OF ATTORNEY IN ORIGINAL APPLICATION

(Sole or Joint - Foreign)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

METHOD OF ANALYZING ELECTROMAGNETIC INTERFERENCE,

the specification of which

XX is attached hereto.

___ was filed on _____ as application Serial No. _____ and was amended on _____.

I hereby state that I have reviewed and understand the content of the above-identified specification, including the claims (Pearne, Gordon, McCoy & Granger Docket No. 32809), as amended by any amendment referred to above. I acknowledge my duty to disclose information of which I am aware which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119, of any foreign application(s) for patent or inventor's certificate listed below, and have also identified below any foreign applications for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Country	Application Number	Filing Date (day/month/year)	Priority Claimed? Yes	No
Japan	P.Hei.11-200847	14/July/1999	XX	

I hereby designate the following as my mailing address and telephone number:

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and appoint each of the following as my attorneys with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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